CLAIMS

1. A row driver adapted to receive an input signal and a test mode signal, and adapted to be coupled to first and second voltage sources and having an output adapted to be coupled to a word line, the row driver operable in an active mode responsive to the test mode signal going inactive to couple the output to either the first or second voltage source responsive to the input signal, and being operable in a standby mode responsive to the test mode signal going active to present a high impedance to the word line.

2. The row driver of claim 1 wherein the first voltage source comprises a supply voltage source and the second voltage source comprises a reference voltage source.

3. The row driver of claim 1 wherein the test mode signal goes active during a standby mode of operation and goes inactive during a normal operating mode during which memory cells coupled to the word line may be accessed.

4. The row driver of claim 1 further comprising:

a first output circuit having a first terminal adapted to receive a supply voltage, a second terminal coupled to an output node, and a control terminal adapted to receive an input signal, the first output circuit being operable to couple the first signal terminal to the second signal terminal responsive to the input signal having a first logic state, and operable to isolate the first and second signal terminals responsive to the input signal having a second logic state;

a second output circuit having a first terminal, a second terminal coupled to the output node, and a control terminal adapted to receive the input signal, the second output circuit being operable to couple the first signal terminal to the second signal

terminal responsive to the input signal having the second logic state, and operable to isolate the first and second signal terminals responsive to the input signal having the first logic state; and

an isolation circuit adapted to receive the reference voltage and coupled to the first terminal of the second output circuit, and adapted to receive a test mode signal, the isolation circuit operable responsive to the test mode signal being inactive to apply the reference voltage on the first terminal of the second output circuit, and operable responsive to the test mode signal being active to present a high impedance on the first terminal of the second output circuit.

5. The row driver of claim 4 wherein the first output circuit comprises a PMOS transistor and the second output circuit comprises an NMOS transistor.

6. The row driver of claim 4 wherein the isolation circuit comprises a transistor.

7. A row driver, comprising:

a PMOS transistor having a source adapted to receive a supply voltage, a gate adapted to receive an input signal, and a drain adapted to be coupled to a word line;

an NMOS transistor having a drain coupled to the drain of the PMOS transistor, a source, and a gate coupled to the gate of the PMOS transistor;

an isolation circuit coupled to the source of the NMOS transistor and adapted to receive a reference voltage and a test mode signal, the isolation circuit coupling the source of the NMOS transistor to the reference voltage responsive to the test mode signal going inactive and presenting a high impedance at the source of the NMOS transistor responsive to the test mode signal going active.

8. The row driver of claim 7 wherein the test mode signal goes active during a standby mode of operation and goes inactive during a normal operating mode during which memory cells coupled to the word line may be accessed.

9. The row driver of claim 7 wherein the reference voltage comprises ground.

10. The row driver of claim 7 wherein the isolation circuit comprises a transistor.

11. A row driver including a PMOS transistor coupled between a supply voltage source and an output node, and including an NMOS transistor coupled between the output node and a reference node, the gates of the transistors being adapted to receive an input signal and the output node being coupled to a word line, and the row driver including an isolation circuit coupled to the reference node and adapted to receive a test mode signal and a reference voltage, the isolation circuit operable in a first mode responsive to the test mode signal going inactive to apply the reference voltage on the reference node and the PMOS and NMOS transistors being operable during the first mode to couple the word line to either the supply voltage or the reference voltage in response to the input signal, and the isolation circuit operable in a second mode responsive to the test mode signal going active to isolate the reference node, the PMOS transistor being deactivated during the second mode and the NMOS transistor being activated to couple the word line to the isolated reference node, the isolated reference node reducing any gate induced leakage current through the PMOS transistor during the second mode.

12. The row driver of claim 11 wherein the test mode signal goes active during a standby mode of operation and goes inactive during a normal operating mode during which memory cells coupled to the word line may be accessed.

13. The row driver of claim 11 wherein the reference voltage comprises ground.

14. A row driver, comprising:

a first coupling means having a first terminal adapted to receive a supply voltage, a second terminal coupled to an output node adapted to be coupled to a word line, and a control terminal adapted to receive an input signal for coupling or isolating the first and second signal terminals responsive to the input signal;

a second coupling means having a first terminal, a second terminal coupled to the output node, and a control terminal adapted to receive the input signal for coupling or isolating the first and second signal terminals responsive to the input signal; and

an isolation means adapted to receive the reference voltage and coupled to the first terminal of the second coupling means, and adapted to receive a test mode signal for applying the reference voltage on the first terminal of the second coupling means when the test mode signal goes inactive and for presenting a high impedance on the first terminal of the second coupling means when the test mode signal goes active.

15. The row driver of claim 14 wherein the test mode signal goes active during a standby modeand goes inactive during a normal operating mode during which memory cells coupled to the word line may be accessed.

16. The row driver of claim 14 wherein the reference voltage comprises ground.

17. A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; the memory-cell array including a plurality of word lines; and

a plurality of row drivers, each row driver coupled to an associated word line in the memory-cell array and coupled to the address decoder to receive a row activation signal, and the row driver being coupled to the control circuit to receive a test mode signal, each row driver being operable in an active mode responsive to the test mode signal going inactive to couple the associated word line to either a first or a second voltage source responsive to the corresponding row activation signal, and being operable in a standby mode responsive to the test mode signal going active to present a high impedance to the corresponding word line.

18. The memory device of claim 17 wherein the first voltage source comprises a supply voltage source and the second voltage source comprises a reference voltage source.

19. The memory device of claim 17 wherein the memory device comprises a flash memory and wherein the test mode signal goes active during a standby mode of operation and goes inactive during a normal operating mode during which memory cells coupled to an addressed word line may be accessed.

20. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising,

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; the memory-cell array including a plurality of word lines; and

a plurality of row drivers, each row driver coupled to an associated word line in the memory-cell array and coupled to the address decoder to receive a row activation signal, and the row driver being coupled to the control circuit to receive a test mode signal, each row driver being operable in an active mode responsive to the test mode signal going inactive to couple the associated word line to either a first or a second voltage source responsive to the corresponding row activation signal, and being operable in a standby mode responsive to the test mode signal going active to present a high impedance to the corresponding word line.

21. The computer system of claim 20 wherein the first voltage source comprises a supply voltage source and the second voltage source comprises a reference voltage source.

22. The computer system of claim 20 wherein the memory device comprises a flash memory and wherein the test mode signal goes active during a standby mode of operation and goes inactive during a normal operating mode during which memory cells coupled to an addressed word line may be accessed.

23. A method of operating a memory device including a memory-cell array having a plurality of memory cells arranged in rows and columns, each memory cell in a respective row being coupled to an associated word line, the method comprising detecting a first mode of operation of the memory device and floating at least some of the word lines when the first mode is detected.

24. The method of claim 23 wherein the first mode comprises a low-power mode of the memory device.

25. The method of claim 24 wherein the memory device comprises a flash memory and wherein the low-power mode comprises a reset/deep power down mode.

26. A method of operating a flash memory device during a standby mode of operation, the flash memory device including a memory-cell array having a plurality of memory cells arranged in rows and columns, each memory cell in a respective row being coupled to an associated word line, the method comprising:

detecting an active mode of operation of the memory device;

during the active mode of operation,

receiving addresses corresponding to memory cells to be accessed,

applying a first voltage to the word line of addressed memory cells to access the memory cells in the corresponding row, and

applying a second voltage to each word line associated with memory cells not being accessed;

detecting a standby mode of operation; and

during the standby mode of operation, isolating at least some of the word lines from the second voltage.

27. The method of claim 26 wherein detecting an active mode of operation comprise detecting a standby mode.

28. The method of claim 26 wherein all the word lines are isolated during the standby mode.

29. The method of claim 26 wherein isolating at least some of the word lines from the second voltage comprises presenting a high impedance between the word line and a source of the second voltage.

30. The method of claim 26 wherein the first voltage comprises a supply voltage and wherein the second voltage comprises ground.